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 Terms used **bipartite** and **worst case** and **aggressor** and **exclusiv** and **noise** or **cross walk**

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21 [Estimation of signal arrival times in the presence of delay noise](#)

Sarvesh Bhardwaj, Sarma B. K. Vrudhula, David Blaauw

 November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design**

 Full text available: pdf(159.61 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Delay due to capacitive coupling of interconnects has become an important reliability issue in the design of nanometer circuits. In this paper we present a probabilistic approach towards analyzing the impact of capacitive coupling noise on signal delay. The variation in the delay is due to the variation in the relative arrival times of the aggressors and the victim. We derive expressions for the moments of the victim voltage in the presence of noise. From these we compute estimates of the earlie ...

22 [Calculating worst-case gate delays due to dominant capacitance coupling](#)

Florentin Dartu, Lawrence T. Pileggi

 June 1997 **Proceedings of the 34th annual conference on Design automation conference**

 Full text available: pdf(98.15 KB) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

23 [Cross-talk noise analysis and management: Variable frequency crosstalk noise analysis: a methodology to guarantee functionality from dc to \$f_{max}\$](#)

Byron Krauter, David Widiger

 June 2002 **Proceedings of the 39th conference on Design automation**

 Full text available: pdf(102.66 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

One means of reducing pessimism in crosstalk analysis is to consider timing orthogonality. While earlier works have addressed the temporal alignment of timing windows [1, 2, 3, 4], these treatments have overlooked one key point. Crosstalk noise failures are frequency dependent. A chip that functions at one frequency can fail due to crosstalk noise at faster and slower frequencies. Moreover, because system developers and manufacturers need chips that operate over a wide range of frequencies, noise ...

Keywords: GCD frequency, LCM window, crosstalk, frequency-dependent noise, noise analysis, timing orthogonality, timing windows

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24 Closed-Form Crosstalk Noise Metrics for Physical Design Applications

L. Chen, M. Marek-Sadowska

March 2002 **Proceedings of the conference on Design, automation and test in Europe**Full text available:  [pdf\(249.22 KB\)](#)Additional Information: [full citation](#), [abstract](#) [Publisher Site](#)

In this paper we present efficient closed-form formulas to estimate capacitive coupling-induced crosstalk noise for distributed RC coupling trees. The efficiency of our approach stems from the fact that only the five basic operations are used in the expressions: addition ($x + y$), subtraction ($x - y$), multiplication ($x \times y$), division (x / y) and square root (\sqrt{x}). The formulas do not require exponent computation or numerical iterations. We have developed closed-form expressions for the peak crosstalk ...

25 Towards true crosstalk noise analysis

Pinhong Chen, Kurt Keutzer

November 1999 **Proceedings of the 1999 IEEE/ACM international conference on Computer-aided design**Full text available:  [pdf\(123.25 KB\)](#)Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Accurate noise analysis is currently of significant concern to high-performance designs, and the number of signals susceptible to noise effects will certainly increase in smaller process geometries. Our approach uses a combination of temporal and functional information to eliminate false transition combinations and thereby overcome insufficiencies in static noise analysis. A similar idea arises in timing analysis where functional and timing information is used to eliminate false paths. The ...

26 Noise propagation and failure criteria for VLSI designs

V. Zolotov, D. Blaauw, S. Sirichotiyakul, M. Becer, C. Oh, R. Panda, A. Grinshpon, R. Levy

November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design**Full text available:  [pdf\(237.68 KB\)](#)Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Noise analysis has become a critical concern in advanced chip designs. Traditional methods suffer from two common issues. First, noise that is propagated through the driver of a net is combined with noise injected by capacitively coupled aggressor nets using linear summation. Since this ignores the non-linear behavior of the driver gate the noise that develops on a net can be significantly underestimated. We therefore propose a new linear model that accurately combines propagated and injected noise ...

27 Cross-talk noise analysis and management: Crosstalk noise estimation for noise management

Paul B. Morton, Wayne Dai

June 2002 **Proceedings of the 39th conference on Design automation**Full text available:  [pdf\(288.08 KB\)](#)Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

One of the main challenges in developing an effective crosstalk noise management strategy is to develop a crosstalk noise estimate which is both accurate and leads to a tractable optimization problem that can be used to optimally redistribute uncommitted routing resources to resolve crosstalk noise violations. Devgan's [4] estimate comes very close to meeting these objectives, however, it is extremely pessimistic for nets with long couplings or aggressor nets with short rise times. The increased ...

Keywords: crosstalk, estimation, local approximation, noise, noise management, optimal


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28 Poster Paper Introductions: Incremental delay change due to crosstalk noise

Lauren Hui Chen, Malgorzata Marek-Sadowska

April 2002 **Proceedings of the 2002 international symposium on Physical design**


Full text available:  [pdf\(124.05 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

In this paper we present efficient closed-form formulas to estimate the incremental delay change induced by capacitive interconnect coupling. We also analyze temporal correlations among switching signals and develop criteria for timing window alignment. Our approximations are conservative and yet achieve acceptable accuracy. The formulas are simple enough to be used in the inner loops of static timing analysis.

29 Cross-talk noise analysis and management: Estimation of the likelihood of capacitive coupling noise

Sarma B. K. Vrudhula, David Blaauw, Supamas Sirichotiyakul

June 2002 **Proceedings of the 39th conference on Design automation**

Full text available:  [pdf\(970.85 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)


The corruption of signals due to capacitive and inductive coupling of interconnects has become a significant problem in the design of deep submicron circuits (DSM). Noise simulators, based on worst-case assumptions, are overly pessimistic. As a result, when they are used on industrial ICs with hundreds of thousands of nets, thousands of nets are reported as having potential noise violations. There is a need to prioritize the problem nets based on the likelihood of the noise and possibly even eli ...

Keywords: deep submicron, noise, signal integrity

30 Novel design methodologies and signal integrity: Temporofunctional crosstalk noise analysis

Donald Chai, Alex Kondratyev, Yajun Ran, Kenneth H. Tseng, Yosinori Watanabe, Malgorzata Marek-Sadowska

June 2003 **Proceedings of the 40th conference on Design automation**

Full text available:  [pdf\(177.56 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)


Noise affects circuit operation by increasing gate delays and causing latches to capture incorrect values. This paper proposes a method of characterizing correlation of signal transitions in multiple nets by considering both timing and functionality of the signals, and uses it in an analysis procedure to eliminate noise faults that cannot actually happen when such correlations are considered. It uses four-variable Boolean logic to characterize signal transitions in a time interval, and formulate ...

Keywords: SAT formula, crosstalk noise, timed Boolean logic

31 Session 9D: Interconnect analysis and extraction: Practical considerations in RLCK crosstalk analysis for digital integrated circuits

Steven C. Chan, K. L. Shepard

November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**

Full text available:  [pdf\(267.95 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Inductance and inductive crosstalk has become an important new concern for on-chip wires

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